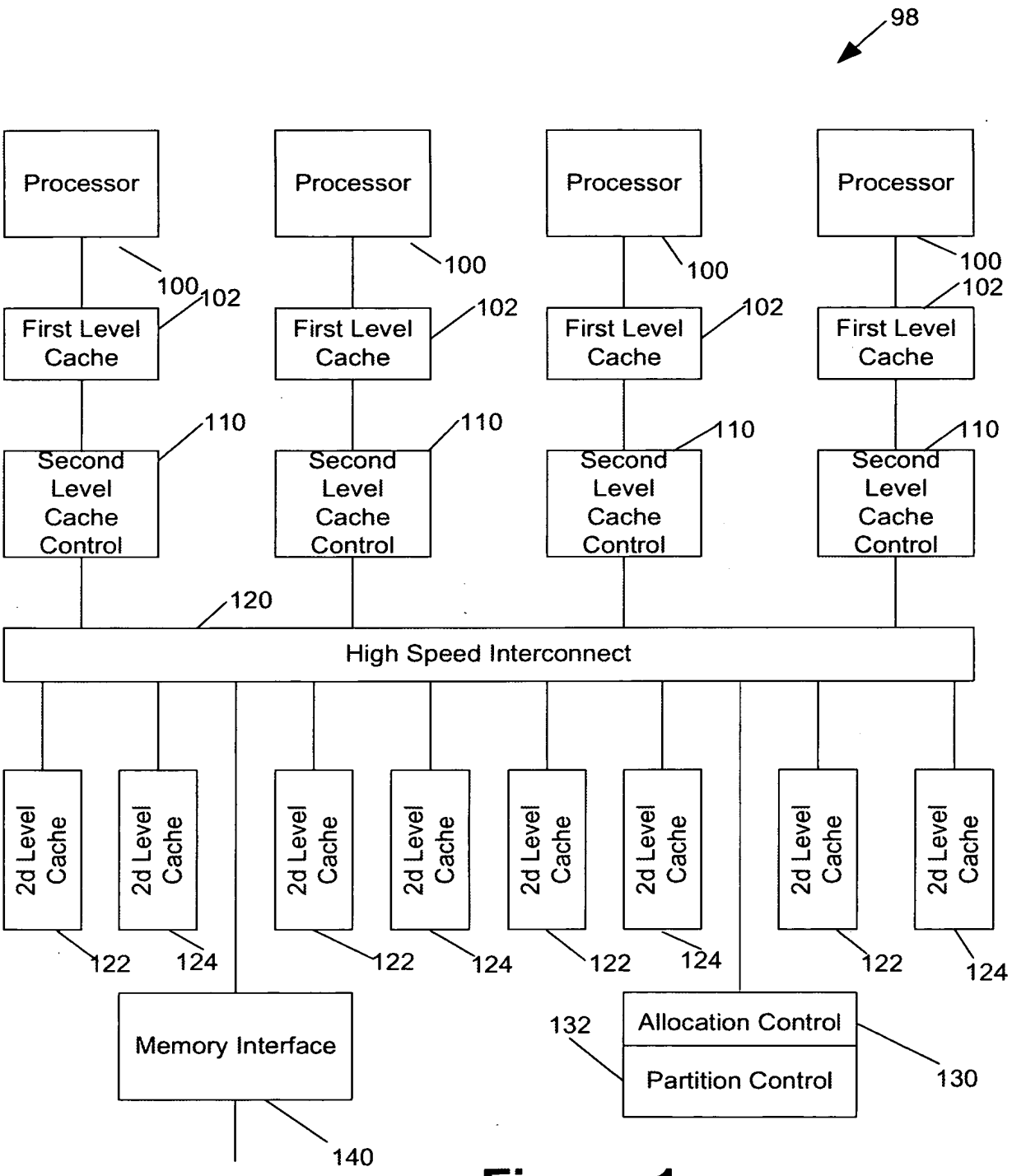
98
Processor
Processor
Processor
Processor
100
100
100
100
102
102
102
102
First Level Cache
First Level Cache
First Level Cache
First Level Cache
110
110
110
110
Second Level Cache Control
Second Level Cache Control
Second Level Cache Control
Second Level Cache Control
120
High Speed Interconnect
2d Level Cache
2d Level Cache
2d Level Cache
2d Level Cache
2d Level Cache
2d Level Cache
2d Level Cache
2d Level Cache
122
124
122
124
122
124
122
124
Memory Interface
Allocation Control
Partition Control
132
130
140

Figure 1

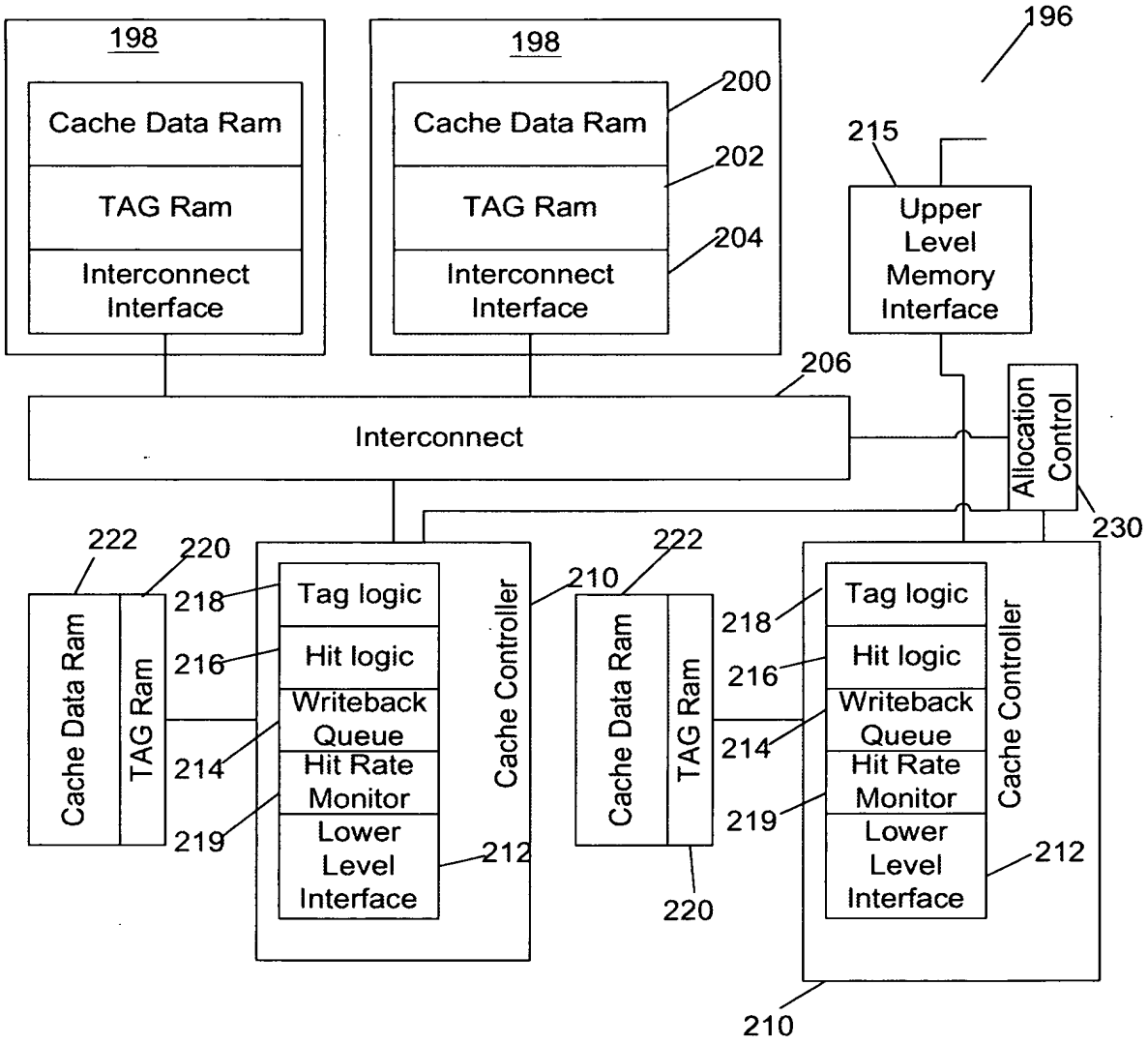
198
198
196
Cache Data Ram
TAG Ram
Interconnect Interface
Cache Data Ram
TAG Ram
Interconnect Interface
200
202
204
215
Upper Level Memory Interface
206
Interconnect
Allocation Control
230
222
220
218
216
214
219
Cache Data Ram
TAG Ram
Tag logic
Hit logic
Writeback Queue
Hit Rate Monitor
Lower Level Interface
Cache Controller
212
210
222
210
218
216
214
219
Cache Data Ram
TAG Ram
220
Tag logic
Hit logic
Writeback Queue
Hit Rate Monitor
Lower Level Interface
Cache Controller
212
210

Figure 2

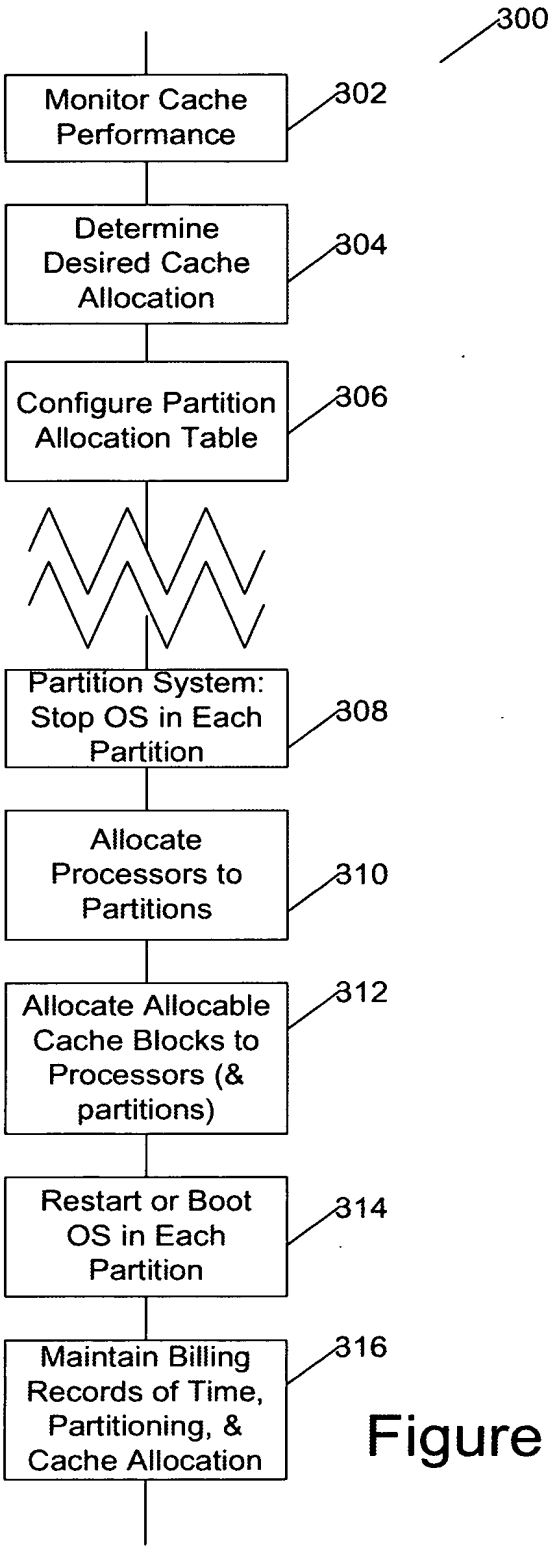
300
Monitor Cache Performance
302
Determine Desired Cache Allocation
304
Configure Partition Allocation Table
306
Partition System: Stop OS in Each Partition
308
Allocate Processors to Partitions
310
Allocate Allocable Cache Blocks to Processors (& partitions)
312
Restart or Boot OS in Each Partition
314
Maintain Billing Records of Time, Partitioning, & Cache Allocation
316

Figure 3